REMARKS

Claims 1-13 presented for examination have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA).

This rejection is respectfully traversed for the following reasons.

In the application of a rejection under 35 U.S.C. § 103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. As stated in ***Graham v. John Deere Co.*** 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. § 103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art. It is respectfully submitted that the Examiner has failed to ascertain the differences between the prior art and the claims in issue.

In particular, claim 1 recites a bi-directional bus circuitry shared among a plurality of circuit blocks. The bus circuitry comprises:

- a data bus divided into (J+1) (J: natural number being 1 or more than 1) bus nodes, each of the plurality of circuit blocks being connected to one of the (J+1) bus nodes;

- a potential fixing circuit provided corresponding to one of the (J + 1) bus nodes, for setting potential level of corresponding the bus node to a prescribed potential when data is input to/output from none of the plurality of circuit blocks;

- J repeater circuits provided between adjacent the bus nodes respectively, each repeater circuit having a first signal transmitting circuit transmitting data from one to the other of the adjacent bus nodes, and a second signal transmitting circuit transmitting data from the other to the one of the adjacent bus nodes; and

- an arbiter circuit receiving circuit block information for specifying a circuit block which

is an object of data output, and controlling activation of the first and second signal transmitting circuits.

Claim 1 specifies that the arbiter circuit activates, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely.

Independent claim 10 recites that the arbiter circuit activates both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used, that is, when data is input to/output from none of the plurality of circuit blocks.

The Examiner holds the arrangement in FIG. 9 of the present application to differ from the claimed invention only in that FIG. 9 does not show the arbiter circuit activating, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely. FIG. 10 is relied upon for showing this element.

The Examiner takes the position that page 3, lines 16-25 of the specification and FIG. 10 suggests activating, when the data is input to/output from none of the plurality of circuit blocks, a signal transmitting circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely.

The Examiner's position is respectfully traversed. As demonstrated below, the background section of the present application provides no support for the Examiner's position.

The specification on page 3, lines 15-33, indicates, in connection with the arrangement in FIG. 9, that "with the potential level of the bus node being unfixed, the potential level of the bus

node comes to be the intermediate potential, possibly causing a constant current, which will be consumed wastefully, in the input and output buffers of the circuit blocks which are connected to the bus node. If the potential of the bus node should be higher than a power supply potential, which corresponds to the H level potential of the data or lower than the ground potential which corresponds to the L level potential of the data because of a noise or the like, there is a possibility of circuit break down in the input and output buffers of the circuit blocks connected to the bus node. Japanese Patent Laying-Open No. 63-85852 proposes a solution to this problem of unfixed potential level of the data bus, which solution provides a bus circuitry configuration allowing fixing of the bus potential when the bus is not used. Fig. 10 is a schematic diagram of a conventional bus circuitry allowing fixing of the bus potential when not in use."

The arrangement in FIG. 10 does not include a circuit for specifying a circuit block which is an object of data output, and controlling activation of a signal transmitting circuit. Hence, none of the elements in FIG. 10 may be considered to correspond to the arbitration circuit of claim 1.

Further, neither the portion of the specification discussed above, nor FIG. 10 suggests activating, when the data is input to/output from none of the plurality of circuit blocks, a signal transmitting circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely, as claim 1 recites. Instead, the disclosure relating to FIG. 10 suggests that "even when all the tristate buffers for providing corresponding data are set to the high-impedance state and bus line BUS is not used, it is possible to fix the potential level of bus line BUS at a prescribed potential level, in this example at the ground potential" (page 4, lines 12-16).

Moreover, the Examiner should recognize that the fact that the prior art *could* be

modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using applicant's claims as a guide. ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Applicant respectfully submits that the Examiner's conclusion of obviousness is based on his inaccurate interpretation of the Applicant's disclosure rather than on the prior art suggestion.

The specification of the present application indicates that "it is difficult to apply the technique for fixing the bus potential when not in use shown in Fig. 10, directly to a bi-directional bus circuitry" (page 4, lines 18-20). It is noted that while FIG. 10 shows a mono-directional bus circuit, FIG. 9 shows the bi-directional bus circuitry.

Accordingly, the background section of the specification expressly **teaches away** from modifying the arrangement in FIG. 9 by incorporating the arrangement in FIG. 10, thereby constituting further **evidence of nonobviousness**. ***In re Bell***, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); ***In re Hedges***, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); ***In re Marshall***, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).

Further, independent claim 10 requires the arbiter circuit to activate both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used. The Examiner did not address this limitation.

However, neither FIG. 9 nor FIG. 10 teaches or suggests activating both of the signal transmitting circuits in each of the repeater circuits when the data bus is not used.

It is well settled that the test for obviousness is what the combined teachings of the

references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of *prima facie* obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the combined teachings relating to FIGS. 9 and 10 of the present application are not sufficient to arrive at the inventions claimed in independent claims 1 and 10. Therefore, the Examiner's conclusion of obviousness is not warranted. Accordingly, the rejection of claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) is improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-13 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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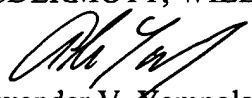

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